# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/774,313 | 02/06/2004 | Benoit Durand | 852663.407 | 5411 |

38106 7590 05/31/2006

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVENUE, SUITE 6300
SEATTLE, WA 98104-7092

| EXAMINER | |
|---|---|
| CONNOLLY, MARK A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2115 | |

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/774,313 | DURAND ET AL. | |
| | Examiner | Art Unit | |
| | Mark Connolly | 2115 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,12-22 and 25* is/are rejected.

7)☒ Claim(s) *9,11,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-25 have been presented for examination.

### *Drawings*

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 14 recites the limitation "the third operating mode" in line 3. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, "the third operating mode" has been interpreted as "a third operating mode."

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-8, 10, 12-22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art [AAPA] in view of Kosuda et al [Kosuda] US Pub 2003/0070106 A1.

7. Referring to claim 1, AAPA teaches the integrated circuit [IC] substantially including:

a. a main oscillator circuit supplying a first clock signal [page 1 lines 12-14].

b. a peripheral circuit supplying a periodic wake-up signal [page 2 lines 1-6].

c. a central processing unit [CPU] having a first operating mode at full power, in which the first clock signal is applied to the central processing unit; an active halt mode, in which the main oscillator circuit and the CPU are deactivated, the central processing unit being awakened by the periodic wake-up signal [page 2 line 15- page 3 line 10].

Although the AAPA teaches the oscillator, peripheral circuit and CPU above, it does not explicitly teach:

d. a secondary oscillator circuit for supplying a second clock signal of lower frequency than the first clock signal

e. a circuit for managing clock signals arranged for, upon the wake-up of the CPU at the end of the active halt mode, waking up the secondary oscillator circuit and applying the second clock signal to the CPU so as to clock the central processing unit to the frequency of the second clock signal and thus obtain a second operating mode with reduced current consumption relative to the first operating mode

Rather, the AAPA teaches waking then applying the first clock signal to the CPU upon wake-up of the CPU at the end of an active halt mode [page 3 lines 11-17]. Kosuda teaches initiating a processing mode by waking and applying a secondary oscillator circuit for supplying

a second clock of lower frequency than a first clock signal which operates the system at a lower power consumption than that using the first clock [¶'s 0105-0106, 0125-0133 and 0151]. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Kosuda into the AAPA system because it would provide a means for waking the CPU in a low power mode and additionally allow the CPU to wake faster due to the shorter wait time required for the second clock to stabilize. Operating in a lower power mode is interpreted as operating at reduced power consumption.

8. Referring to claims 2 and 3, Kosuda teaches initiating the CR oscillating circuit (i.e. secondary oscillator) first without the PLL oscillating circuit (i.e. main oscillator) then starting the PLL afterwards [¶0235].

9. Referring to claims 4 and 5, Kosuda teaches waking the main oscillator and deactivating the secondary oscillator circuit when applying the first clock signal [¶0129-0135].

10. Referring to claim 6, Kosuda teaches transitioning from the CR clock to the PLL clock [CLK2 fig. 15]. At no time is there an instance where CLK2 is absent. Therefore it is interpreted that all devices being clocked by the CR/PLL clock would not be interrupted and would continue to operate through the transition.

11. Referring to claim 7, Kosuda teaches being able to wake both the CR and PLL clocks simultaneously [¶0235].

12. Referring to claim 8, Kosuda teaches a switch circuit for supplying either the first or second clock and a control circuit for waking/deactivating a main and secondary oscillator and actuating the switch circuit [¶'s 0128-0135].

13. Referring to claim 10, the AAPA teaches interrupting the CPU and clock signals during a halt mode [page 3 lines 1-10].

14. Referring to claim 12, the AAPA teaches deactivating the clocks only in response to a halt condition [HALT fig. 1 and page 3 lines 1-10].

15. Referring to claim 13, Kosuda teaches flags for waking the main and secondary oscillators and for selecting the transmission of the first or second clock signal [¶'s 0128-0135].

16. Referring to claim 14, the AAPA teaches counting stabilization cycles [page 3 lines 11-17].

17. Referring to claim 15, although in Kosuda it appears that the secondary oscillator (CR) consumes more current than the main oscillator (PLL) [¶'s 0105-0106], it is also explicitly taught that the secondary oscillator could be a quartz oscillator which could consume less current than a PLL oscillator.

18. Referring to claim 16, Kosuda teaches the secondary oscillator with a negligible stabilization time relative to the main oscillator [¶'s 0105-0106].

19. Referring to claim 17, Kosuda teaches the secondary oscillator is a resistance capacitance type [fig. 11].

20. Referring to claim 18, this is rejected on the same basis as set forth hereinabove. In addition, the AAPA teaches a clock management circuit (MUX) which receives a plurality of clock signals and outputs one of the clock signals to the CPU and wakeup circuit which supplies a wake-up signal (IT) to a CPU [fig. 1 and page 3 lines 8-10]. Kosuda teaches initiating an information processing mode which requires selection of a secondary clock. In the AAPA-Kosuda system, because the wake-up circuit determines and controls the systems wake-up and

because it is necessary to select the secondary clock upon initial operation, it would have been obvious to have the wake-up circuit select the secondary clock from the clock management circuit so that it maintains control of the wake-up process.

21. Referring to claim 19, the AAPA teaches an interrupt decode circuit coupled between the clock wakeup circuit and the CPU [fig. 1 and page 2 lines 1-11].

22. Referring to claims 20-22, these are rejected on the same basis as set forth hereinabove.

23. Referring to claim 25, the AAPA teaches maintaining operation of a wakeup clock while the CPU is in a sleep mode [OSCAUX fig. 1 and page 2 lines 3-6].

***Allowable Subject Matter***

24. Claims 9, 11 and 23-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (571) 272-3666. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mark Connolly
Examiner
Art Unit 2115

mc
May 19, 2006

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100